



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/738,986	12/19/2000	Ju Hyun Lee	MRE-002	2706

34610 7590 06/20/2006

FLESHNER & KIM, LLP  
P.O. BOX 221200  
CHANTILLY, VA 20153

EXAMINER

SELBY, GEVELL V

ART UNIT	PAPER NUMBER
----------	--------------

2622

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/738,986

Applicant(s)

LEE, JU HYUN

Examiner

Gevell Selby

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5 and 6 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 December 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burrows et al., US 6,091,838, in view of Li et al., US 6,219,793.**

In regard to claim 1, Burrows et al., US 6,091,838, discloses a fingerprint recognition system comprising:

an image sensor (see figure 1, element 150 and column 6, lines 28-33);

a transparent electrode thin film (see figure 1, element 104 and 105 in combination) at an upper portion of the image sensor (see column 4, line 62 to column 5, line 1), one terminal of an AC power source being connected with said transparent electrode layer (see column 5, lines 2-3);

a luminescent layer (see figure 1, element 103) formed on the transparent electrode layer, said luminescent layer having fluorescent particles and a binder (see column 5, lines 39-47);

a dielectric layer (see figure 1, element 102) formed at an upper portion of the luminescent layer (see column 5, lines 26-30); and

a contamination-resistance film (see figure 1, element 107) formed at an upper portion of the dielectric layer (see column 5, lines 16-25 and 40-43).

The Burrows reference does not disclose that the image sensor is a CMOS image sensor.

Li et al., US 6,219,793, discloses a fingerprint recognition system wherein the imager is a CCD array or a CMOS photodiode/photogate array to generate an electronic image of the user's fingerprint (see column 12, lines 43-46). It teaches that if a CMOS sensor is used, it may be provided on a single integrated circuit together with processing logic such as a CPU (see column 12, lines 46-48)

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Burrows et al., US 6,091,838, in view of Li et al., US 6,219,793, to have a CMOS image sensor, in order to capture an electronic image of high quality to be processed for recognition by a CPU on the same substrate, which makes the system more compact while provide high image quality.

In regard to claim 2, Burrows et al., US 6,091,838, in view of Li et al., US 6,219,793, discloses the fingerprint recognition sensor according to claim 1. The Burrows reference discloses wherein the transparent electrode layer is directly deposited as a thin film on the CMOS image sensor (see column 4, line 66 to column 5, line 1).

In regard to claim 1, Burrows et al., US 6,091,838, discloses a method for manufacturing a fingerprint recognition sensor, comprising the steps of:

providing an image sensor (see figure 1, element 150 and column 6, lines 28-33);

directly depositing a transparent electrode layer as a thin film at an upper portion of the CMOS image sensor (see figure 1 , elements 104 and 105 in combination and

Art Unit: 2622

column 4, line 66 to column 5 line 1) and connecting one terminal of an AC power source to the transparent electrode layer (see column 5, lines 2-3), said transparent electrode layer being made of a transparent insulating material and a transparent conductive material (see column 4, line 55 to column 6, line 1);

forming a luminescent layer at an upper portion of the transparent electrode layer to generate an optical image (see figure 1, element 103 and column 5, lines 26-30);

forming a dielectric layer at an upper portion of the luminescent layer (see figure 1, element 102 and column 5, lines 26-30); and

forming a contamination-resistance film at an upper portion of the dielectric layer (see figure 1, element 107).

In regard to claim 5, Burrows et al., US 6,091,838, discloses a fingerprint recognition system comprising:

an image sensor (see figure 1, element 150 and column 6, lines 28-33);

a transparent electrode thin film (see figure 1, element 104 and 105 in combination) directly deposited as a thin film at an upper portion of the image sensor (see column 4, line 62 to column 5, line 1); and

a fingerprint recognition sensor is installed at an upper portion of the transparent electrode thin film (see figure 1, element 100 and column 4, lines 49-61).

The Burrows reference does not disclose that the image sensor is a CMOS image sensor.

Li et al., US 6,219,793, discloses a fingerprint recognition system wherein the imager is a CCD array or a CMOS photodiode/photogate array to generate an electronic image of the user's fingerprint (see column 12, lines 43-46). It teaches that if a CMOS sensor is used, it may be provided on a single integrated circuit together with processing logic such as a CPU (see column 12, lines 46-48)

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Burrows et al., US 6,091,838, in view of Li et al., US 6,219,793, to have a CMOS image sensor, in order to capture an electronic image of high quality to be processed for recognition by a CPU on the same substrate, which makes the system more compact while provide high image quality.

In regard to claim 6, Burrows et al., US 6,091,838, in view of Li et al., US 6,219,793, discloses the fingerprint recognition system according to claim 5. Neither reference discloses wherein the CMOS image sensor includes a ground frame having at least one pin.

Official Notice is taken that it well-known in the imaging art for a CMOS image sensor to include a ground frame having at least one pin, in order to secure the image sensor in its place and connect it with the rest of the imaging system so that the system can operate properly and the operate is not interrupted when the system is moved.

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Burrows et al., US 6,091,838, in view of Li et al., US 6,219,793 to have the CMOS image sensor include a ground frame having at least one pin, in order to secure the image sensor in its place and connect it with the rest

of the imaging system so that the system can operate properly and the operate is not interrupted when the system is moved.

*Allowable Subject Matter*

3. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Conclusion*

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,326,644, discloses a contact light emitting device including a transparent electrode layer and a luminescence layer, which can be used in a finger recognition system.

US 6,628,377, discloses a scanning optical semiconductor fingerprint detector that scan the finger as is moves over the array.

US 6,011,859, discloses a solid-state fingerprint sensor packing apparatus with a laminate that seals the device to prevent contamination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 571-272-7369. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

Art Unit: 2622

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

gvs

  
TUAN HO  
PRIMARY EXAMINER